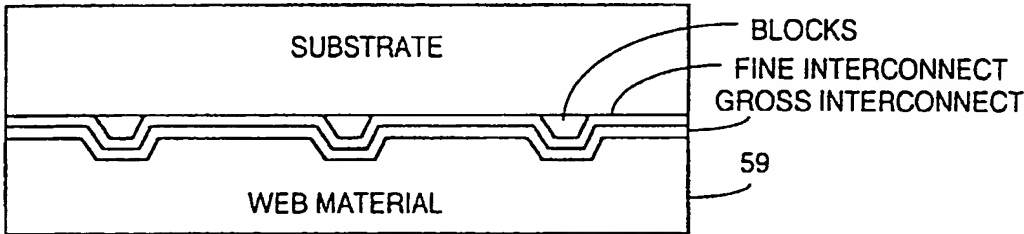


PCTWORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁷ : H01L 23/538, 21/98	A1	(11) International Publication Number: WO 00/55915 (43) International Publication Date: 21 September 2000 (21.09.00)
(21) International Application Number: PCT/US00/02348 (22) International Filing Date: 31 January 2000 (31.01.00) (30) Priority Data: 09/268,755 16 March 1999 (16.03.99) US (71) Applicant (for all designated States except US): ALIEN TECHNOLOGY CORPORATION [US/US]; 900 E. Hamilton Avenue, Suite 100, Campbell, CA 95008 (US). (72) Inventors; and (75) Inventors/Applicants (for US only): JACOBSEN, Jeffrey, Jay [US/US]; 501 Tevis Trail, Hollister, CA 95023 (US). GENDEL, Glenn, Wilhelm [US/US]; 1317 Riverglen Way, Berthoud, CO 80513 (US). HADLEY, Mark, A. [US/US]; 39887 Cedar Boulevard #353, Newark, CA 94560 (US). CRAIG, Gordon, S., W. [US/US]; 1476 Dana Avenue, Palo Alto, CA 93401 (US). SMITH, John, Stephen [US/US]; 1438 Oxford Street, Berkeley, CA 94709 (US). (74) Agents: SCHELLER, James, C., Jr. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).		(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published <i>With international search report.</i>
(54) Title: WEB PROCESS INTERCONNECT IN ELECTRONIC ASSEMBLIES  <p>The diagram is a cross-sectional view of an electronic assembly. It features a top layer labeled 'SUBSTRATE' and a bottom layer labeled 'WEB MATERIAL'. Between these two layers, there is a series of rectangular blocks. These blocks are interconnected by two types of lines: 'FINE INTERCONNECT' and 'GROSS INTERCONNECT'. A specific layer of the gross interconnect is labeled with the reference numeral '59'.</p>		
(57) Abstract <p>Apparatuses and methods for forming displays are claimed. One embodiment of the invention relates to depositing a plurality of blocks onto a substrate and is coupled to a flexible layer having interconnect deposited thereon. Another embodiment of the invention relates to forming a display along a length of a flexible layer wherein a slurry containing a plurality of elements with circuit elements thereon washes over the flexible layer and slides into recessed regions or holes found in the flexible layer. Interconnect is then deposited thereon. In another embodiment, interconnect is placed on the flexible layer followed by a slurry containing a plurality of elements.</p>		

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece			TR	Turkey
BG	Bulgaria	HU	Hungary	ML	Mali	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MN	Mongolia	UA	Ukraine
BR	Brazil	IL	Israel	MR	Mauritania	UG	Uganda
BY	Belarus	IS	Iceland	MW	Malawi	US	United States of America
CA	Canada	IT	Italy	MX	Mexico	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NE	Niger	VN	Viet Nam
CG	Congo	KE	Kenya	NL	Netherlands	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NO	Norway	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	NZ	New Zealand		
CM	Cameroon			PL	Poland		
CN	China	KR	Republic of Korea	PT	Portugal		
CU	Cuba	KZ	Kazakhstan	RO	Romania		
CZ	Czech Republic	LC	Saint Lucia	RU	Russian Federation		
DE	Germany	LJ	Liechtenstein	SD	Sudan		
DK	Denmark	LK	Sri Lanka	SE	Sweden		
EE	Estonia	LR	Liberia	SG	Singapore		

WEB PROCESS INTERCONNECT IN ELECTRONIC ASSEMBLIES

BACKGROUND INFORMATION

1. Field of the Invention

The present invention relates generally to the field of fabricating electrical assemblies which include functional blocks that are deposited onto a substrate.

2. Description of Related Art

Various different types of assemblies include functional blocks which are separately fabricated and then are deposited onto receiving regions of a substrate. One such type of an assembly is a display panel. Fabrication of display panels is well known in the art. Display panels may be comprised of active matrix or passive matrix panels. Active matrix panels and passive matrix panels may be either transmissive or reflective. Transmissive displays include polysilicon thin-film transistor (TFT) displays, and high-resolution polysilicon displays. Reflective displays typically comprise single crystal silicon integrated circuit substrates that have reflective pixels.

Liquid crystals, electroluminescent (EL) materials, organic light emitting diodes (OLEDs), up and downconverting phosphor (U/DCP), electrophoretic (EP) materials, or light emitting diodes (LEDs) may be used in fabricating flat-panel display panels. Each of these is known in the art and is discussed briefly below.

Liquid crystal displays (LCDs) can have an active matrix backplane in which thin-film transistors are co-located with LCD pixels. Flat-panel displays employing LCDs generally include five different components or layers: a White or sequential Red, Green, Blue light source, a first polarizing filter, that is

mounted on one side of a circuit panel on which the TFTs are arrayed to form pixels, a filter plate containing at least three primary colors arranged into pixels, and a second polarizing filter. A volume between the circuit panel and the filter plate is filled with a liquid crystal material. This material will rotate the polarized light when an electric field is applied between the circuit panel and a transparent ground electrode affixed to the filter plate or a cover glass. Thus, when a particular pixel of the display is turned on, the liquid crystal material rotates polarized light being transmitted through the material so that it will pass through the second polarizing filter. Some liquid crystal materials, however, require no polarizers. LCDs may also have a passive matrix backplane which is usually two planes of strip electrodes which sandwich the liquid crystal material. However, passive matrices generally provide a lower quality display compared to active matrices. U/DCP and EP displays are formed in a similar fashion except the active medium is different (*e.g.*, upconverting gas, downconverting gas, electrophoretic materials).

EL displays have one or more pixels that are energized by an alternating current (AC) that must be provided to each pixel by row and column interconnects. EL displays generally provide a low brightness output because passive circuitry for exciting pixel phosphors typically operates at a pixel excitation frequency that is low relative to the luminance decay time of the phosphor material. However, an active matrix reduces the interconnect capacitance allowing the use of high frequency AC in order to obtain more efficient electroluminescence in the pixel phosphor. This results in increased brightness in the display.

LED displays are also used in flat-panel displays. LEDs emit light when energized. OLEDs operate like the LEDs except OLEDs use organic material in the formation of the diode.

Regardless of the type of active medium used, displays are generally comprised of at least a substrate and a backplane. The backplane forms the

electrical interconnection of the display and comprises electrodes, capacitors, and transistors in at least some embodiments of a backplane.

Figure 1A illustrates a rigid display device wherein the active matrix display backplane 10 is coupled to a rigid substrate 12. Typically, the active matrix display backplane is also rigid. **Figure 1B** shows another rigid display. There, the active matrix display backplane 10 is coupled to a rigid substrate 12 (*e.g.*, glass). Also shown is a plurality of blocks 14. These blocks may be fabricated separately and then deposited into holes on substrate 12 by a process known as fluidic self assembly (FSA); an example of this process is described in U.S. Patent 5,545,291. These blocks may each contain driver circuitry (*e.g.*, MOSFET and capacitor) for driving a pixel electrode. The active matrix backplane includes transparent pixel electrodes and row/column interconnects (not shown) to electrically interconnect the blocks 14. The plurality of blocks 14 is coupled to the active matrix display backplane 10 and the rigid substrate 12. **Figure 1C** shows a reflective display 16 coupled to a rigid substrate 12. **Figure 1D** shows a reflective display 16 coupled to a rigid substrate 12. A plurality of blocks 14 is coupled to the reflective display 16 and to the rigid substrate 12.

Placing elements, such as pixel drivers, on a rigid substrate is well known. Prior techniques can be generally divided into two types: deterministic methods or random methods. Deterministic methods, such as pick and place, use a human or robot arm to pick each element and place it into its corresponding location in a different substrate. Pick and place methods generally place devices one at a time and are generally not applicable to very small or numerous elements such as those needed for large arrays, such as an active matrix liquid crystal display.

Random placement techniques are more effective and result in high yields if the elements to be placed have the right shape. U.S. Patent No. 5,545,291 describes a method that uses random placement. In this method, microstructures are assembled onto a different substrate through fluid transport.

-4-

This is sometimes referred to as fluidic self-assembly. Using this technique, various blocks, each containing a functional component, may be fabricated on one substrate and then separated from that substrate and assembled onto a separate rigid substrate through the FSA process. The blocks which are deposited onto receptor regions of a substrate may include any of a number of different functional components, such as LEDs, pixel drivers, sensors, *etc.* An example of a particular type of block and its functional component is described in copending US patent application serial number 09/251,220 which was filed Feb. 16, 1999 by the inventor John Stephen Smith and which is entitled "Functionally Symmetric Integrated Circuit Die". This application is hereby incorporated herein by reference.

As noted above, **Figures 1B and 1D** illustrate a display substrate 12 with blocks 14 formed in the rigid substrate 12. These blocks 14 may be deposited through an FSA process. In the FSA process, a slurry containing the blocks 14 is deposited over the rigid substrate 12 and the blocks 14 rest in corresponding openings in the substrate 12.

Figure 2 shows a block 14 and a circuit element (not shown) on the top surface 18 of block 14. Generally, blocks 14 have a trapezoidal cross-section where the top of the block is wider than the bottom of the block 14.

Figure 3 shows block 14 in a recessed region of the rigid substrate 12. Between the block 14 and the rigid substrate is an eutetic layer 13. The block 14 has a top surface 18.

Figure 4 shows a planar side view of a rigid substrate coupled to a rigid display backplane with a plurality of blocks between the display backplane 30 and substrate 12. The plurality of blocks are functionally part of the display backplane 30 and are deposited onto receptor regions of the substrate 12. Each block drives at least one transparent pixel electrode. The pixel electrode is fabricated over a transistor which is fabricated in the block.

Figure 5 shows a portion of an array in an active matrix display backplane. The control line rows 31 and 32 in this device are coupled to gate electrodes along a row and the control line columns 34 and 35 are coupled to data drivers which supply pixel voltages which are applied to the pixel electrodes. A column line 34 is connected to a source electrode of field effect transistor (FET) 36. Another column line 35 is coupled to a source electrode of FET 37. A row line 32 is coupled to the gates of both FETs 36 and 37. The drain of FET 36 is coupled through capacitor 38 to a transparent pixel electrode along the row 32 formed by FETs 36 and 37, and the drain of FET 37 is coupled through a capacitor to another pixel electrode along the row. In one typical example, the backplane may be formed by depositing blocks, using an FSA technique, into a rigid substrate (*e.g.*, glass); each block contains a FET and a capacitor and is interconnected to other blocks by column and row conductors that are deposited onto the rigid substrate; and, the capacitor is coupled to a pixel electrode by another conductor that is deposited onto the rigid substrate. The active medium (*e.g.*, a liquid crystal) is deposited at least on the pixel electrodes which will optically change the active medium's properties in response to the combined voltages or currents produced by the pixel electrodes. The active medium at a given pixel electrode 42 will appear as a square or dot in the overall checkerboard type matrix of the display. The actual size of the FETs and the pixel electrodes 42 are not now drawn to scale, but are shown schematically for the purposes of illustration.

Several disadvantages exist relative to the related art. Display resolution of a flexible display is limited by the amount of interconnect placed on a flexible substrate. Too much interconnect allowing increased conductance of current could damage a substrate made of plastic. Accordingly, it is desirable to use extensive web process interconnect in a display to increase resolution but avoid the problem of a flexible substrate (*e.g.*, plastic substrate) from being harmed by the interconnect.

BRIEF SUMMARY OF THE INVENTION

The present invention provides apparatuses and methods for creating an assembly with an electrical interconnect. A plurality of blocks are deposited onto a substrate. An interconnect layer is placed onto a flexible layer that is coupled to the substrate.

While an array of components (e.g. display components) for an assembly have been described as examples of the invention, an array of other assemblies such as x-ray detectors, radar detectors, micro-electro-mechanical structural elements (MEMS) or, generally, an assembly of sensors or actuators or an assembly of circuit elements also may be produced using the claimed invention. Thus, for example, flexible antennas, other sensors, detectors, or an array of circuit elements may be fabricated using one of the embodiments of the inventions. Other aspects and methods of the present invention as well as apparatuses formed using these methods are described further below in conjunction with the following figures.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example. The invention is not limited to the figures of the accompanying drawings in which like references indicate similar elements. Note also that the elements in the figures are not drawn to scale.

Figure 1A shows a planar side view of an active matrix display backplane coupled to a rigid substrate.

Figure 1B shows a planar side view of an active matrix display backplane coupled to a rigid substrate wherein a plurality of blocks are part of the active matrix display.

Figure 1C shows a planar side view of a reflective display backplane coupled to a rigid substrate.

Figure 1D shows a planar side view of a reflective display backplane coupled to a rigid substrate wherein a plurality of blocks are coupled to the reflective display and to the rigid substrate.

Figure 2 shows a top side perspective view of a circuit element block.

Figure 3 shows a planar side view of blocks in recessed regions of the rigid substrate and a metalization surface on the blocks.

Figure 4 shows a planar side view of a rigid substrate coupled to a rigid display backplane with a plurality of blocks between the display backplane and substrate.

Figure 5 schematically represents a portion of an array of an active matrix backplane.

Figure 6 shows a top view of a plurality of pixel electrodes in a backplane.

Figures 7A – 7G show an assembly of a display wherein blocks are deposited therein followed by a layer of interconnect. The web material is then coupled to a substrate.

Figure 7H shows a polymer layer in between the interconnect (or dielectric layer) and the web material.

Figure 7I shows a top view of an example of a flexible (“tape”) interconnect layer having a patterned interconnect layer. **Figure 7J** shows a cross-sectional view of the tape of **Figure 7I**.

Figures 8A – 8E show an alternative embodiment of the invention. In this embodiment, interconnect is first deposited on web material followed by blocks that are deposited into recessed regions or holes in the web material.

Figures 9A – 9D show another embodiment of the invention wherein blocks are dispensed onto a web material followed by a layer of interconnect.

Figure 10 shows a flow chart of a method of fabricating a display device wherein a web process interconnect is coupled to a web material.

Figure 11 shows a flow chart of a method of assembling multiple displays using web material with interconnect.

Figures 12A – 12B show another embodiment of the invention in which a reflective display is assembled using web material.

Figure 13 shows a method of fabricating a display device wherein a web material and a substrate undergo processing and are subsequently coupled.

Figure 14 shows the overall process of fabricating a display device wherein a web material and a display tape undergo processing and are subsequently coupled.

Figure 15 relates to a method of picking and placing of objects onto a web material after the FSA process has been applied to the web material.

Figure 16 shows an embodiment of the overall in-line process of the invention.

Figure 17 shows a display material being screen printed.

Figure 18 shows a top view of display material being laser etched.

Figure 19 shows lithography being used to pattern display material.

Figure 20 shows display material being deposited in a pattern.

DETAILED DESCRIPTION

The present invention relates to apparatuses and methods for forming an assembly having a substrate. The following description and drawings are illustrative of the invention and are not to be construed as limiting the invention.

One embodiment has a web material having a plurality of blocks with an interconnect deposited thereon and the web material is subsequently optionally coupled to a substrate. These displays can be made into active matrix display devices or passive matrix displays. These flexible displays can be fitted to an object which is either rigid or flexible and which has a non-planar surface. Another embodiment of the invention relates to interconnect being deposited onto a web material followed by blocks with circuit elements thereon being seated in recessed regions or holes in the web material. Other embodiments of the invention include coupling a web material having blocks to a flexible continuous substrate upon which multiple flexible displays are fabricated. The multiple flexible displays may be of similar or different sizes. These displays are separated from one another as the substrate is advanced through the web processing apparatus. The backplane of the display may be comprised of a plurality of blocks wherein each block has a circuit element thereon. The blocks are contained in a slurry which is deposited onto the flexible substrate. Although blocks may be comprised of single crystal silicon or other like material which makes the block rigid, the substrate may still be flexible because the size of these blocks (50 x 100 microns or 100 x 100 microns) is small in comparison to the flexible substrate. The flexible substrate forms part of a display backplane. The flexible displays may be either an active matrix or a passive matrix displays.

Another embodiment of the invention relates to a flexible substrate with a reflective display backplane that has tape with interconnect deposited thereon.

Incorporated by reference is United States Patent No. 5,545,291 explaining how to assemble microstructures onto a substrate; this process may be referred to said FSA (fluidic self assembly), and this process may be performed with a web material. With certain embodiments of the invention, a web material is advanced through a web process apparatus. The FSA process deposits a plurality of blocks onto the web material wherein the blocks fall into recessed regions found in the web material. The web material is then advanced to a further point in the process wherein an interconnect layer is deposited thereon. In one embodiment, the interconnect includes a dielectric layer to provide a multiple layer interconnect. While the web material is advanced, a display tape is advanced to a point wherein the web material becomes coupled to the display tape. This assembly is then coupled to flexible or rigid substrate (or no substrate).

Before the coupling takes place, in certain embodiments interconnect pattern is placed onto the web material that is used to form the backplane. A display material is then deposited onto the display tape. The display material may be cholesteric liquid crystal, polymer-dispersed liquid crystal or other type of material. The display material is layered or patterned on the display tape. The display tape may also include an electrical interconnect (*e.g.* a cover “glass” electrode) and this interconnect may be deposited and/or etched on the display material. This is done by using laser etch, ink jet, screen print, deposit, ultraviolet light (UV) or lithography and etch.

A continuous process as in certain embodiments of the invention offers the advantage of increasing the number of flat-panel displays produced, thereby reducing the cost of manufacturing the displays. FSA in conjunction with a deterministic method of placing blocks (*e.g.*, “pick and place”) with circuit elements of objects onto a web process material is also disclosed. In this aspect of the invention, the recessed regions of the web material are checked for empty regions. If there is an empty recessed region in the web material, an object is

robotically placed into the empty recessed region. The advantage offered by robotically placing an object into an empty recessed region of a web material is that it increases the overall effectiveness and the quality of the displays.

In the following description, numerous specific details such as specific materials, processing parameters, processing steps, *etc.*, are set forth in order to provide a thorough understanding of the invention. One skilled in the art will recognize that these details need not be specifically adhered to in order to practice the claimed invention. In other instances, known processing steps, materials, *etc.* are not set forth in order not to obscure the invention.

Figures 7A – 7F show one embodiment of the invention where blocks are placed onto the web material followed by single or multiple layers of interconnect. **Figure 7A** shows a substrate 59 which may be a flexible web material. **Figure 7B** shows a planar side view of web material 59 having recessed regions or holes therein. These recessed regions or holes may be created by a variety of methods. For example, the recessed regions or holes may be created by a web wheel, roller, or template, that have protruding structures as described in U.S. Patent Application entitled Apparatuses and Methods for Forming Assemblies (Docket No. 003424.P016) by Jeffrey Jay Jacobsen. The hole may be circular in shape but does not separate the web material into pieces. Another method involves using a template having blocks wherein the blocks are pressed into web material 59 making recessed regions or holes into the web material 59 (see U. S. Patent Application entitled “Methods for Transferring Elements From a Template to a Substrate” (Docket No. 003424.P009) describing the donor transfer method). **Figure 7C** shows a planar side view of web material 59 wherein the blocks are seated in the recessed regions or holes. The blocks 14 comprise an active circuit element (not shown) which drives a picture element (not shown). The holes may be used to create an electrical interconnect from one side of the web material to the other side through a conductor in the hole.

Figure 7D shows a planar side view of web material 59 wherein an electrical interconnect is deposited onto the web material 59. Interconnect may be comprised of conductive polymers, metals (*e.g.*, aluminum, copper, silver, gold, *etc.*), metal particles, conductive organic compounds, or conductive oxides. The techniques used for creating Tape Automated Bonding (TAB) tape in the semiconductor industry may be used to create flexible interconnect layers. Numerous methods of depositing interconnect are described in more detail below. The interconnect may be patterned to create an intricate wiring pattern such as row and/or column interconnects for an active matrix display backplane.

It should be noted that web generally involves a roll process is a flexible sheet with very high aspect ratios such as 25:1 or more (length:width). For example, a roll of paper towel when unrolled is said to be in web form and it is fabricated in what is known as a web process. When a web is coiled, it is in a roll form.

Figure 7E shows web material 59 with interconnect 65 deposited thereon. **Figure 7F** shows the web material 59 with interconnect 65 of **Figure 7E** facing a substrate 50. **Figure 7G** shows the web material 59 with interconnect 65 coupled to the substrate 50 of **Figure 7F**. **Figure 7H** shows a web material wherein blocks are deposited into recessed regions or holes found in the web material. A thin polymer layer is deposited on top of the web material and the blocks. This polymer layer may range in thickness from 1 micron to 5 microns. The interconnect layer, in comparison, ranges in thickness from 1,000 angstroms to 1 micron. In one embodiment, vias are formed through the polymer layer and a conductive material such as an aluminum alloy is formed in the vias to connect the blocks to the interconnect.

It will be appreciated that the interconnection pattern (*e.g.* the rows and columns of **Figure 5**) may require either multiple flexible tape layers or a multiple interconnect layer (with dielectric layers between conductive layers) on a flexible tape. The signals from one layer to the next layer are typically

transmitted through vias in the layers. Furthermore, the top interconnect layer will typically provide contact pads to which external circuitry may be coupled. It will also be appreciated that many of the planar side views are not representative of (or illustrating) the actual electrical interconnect pattern which may exist. These actual patterns will depend on the application. **Figures 7I and 7J** show an example of an actual electrical pattern which may be created on a flexible interconnect layer, such as a flexible web tape material. The flexible interconnect layer 1001 may be created from one of numerous types of materials which are appropriate for a web tape material which is designed to hold electrically conductive interconnect layer(s); these materials include polyimide tapes on which are deposited a conductive trace of metal. The metal may be deposited directly on the tape (*e.g.* by a blanket deposition) and then patterned by etching, or a photoresist layer may be applied and patterned, leaving grooves into which metal may be deposited. **Figure 7I** shows a planar top view of a flexible interconnect layer 1001 on which a plurality of row interconnects are created. These row interconnects are electrically similar to the row interconnects (*e.g.* 31 and 32) of **Figure 5**. Each row interconnect, such as row interconnects 1002a or 1002b or 1002n, includes a terminal such as terminal 1003a or terminal 1003b or terminal 1003n, which is used to provide a row signal to all of the contact pads along a row, such as contact pad 1004. It will be appreciated that, in one embodiment in which the interconnect layer 1001 is used in an active material liquid crystal display backplane, the contact pads are coupled to the gates of the FETs (*e.g.* FETs 36 and 37) along a row of the display, and these FETs are disposed in the blocks (*e.g.* block 14) which are deposited by an FSA process into a substrate, such as the substrate 59. It will be understood that in this embodiment, each block with typically include the pixel driving circuitry for a particular pixel in the liquid crystal display, and the flexible interconnect tape 1001 interconnects electrically the gates of the FETs in each block along a row. The interconnect material on the tape 1001 may directly connect to a contact pad on a block or may connect electrically through a via in a tape which is sandwiched between the flexible interconnect tape 1001 and the block 14. The

tape, once created, may be applied to the substrate (or onto another tape on the substrate) in order to electrically interconnect components on the substrate. The tape may also electrically interconnect traces on another tape. It will be appreciated that the flexible interconnect layer 1001 may be fabricated in a web process and then aligned with a substrate having blocks 14 either in a web process or outside of a web process. It will be further appreciated that the substrate may be rigid (and not made in a web process), or the substrate may be flexible and made in a web process. It will also be appreciated that an alignment operation, using conventional techniques, may be necessary to properly align an interconnect tape relative to another interconnect tape, or to a substrate with blocks, when the interconnect tape is coupled to the substrate or to another interconnect tape.

Figure 7J shows a cross-sectional view of the tape 1001, where the cross-section of tape 1001 of **Figure 7I** is taken along the line 7J-7J shown in **Figure 7I**. As shown in **Figure 7J**, a plurality of row interconnects, such as row interconnects 1002a, 1002b and 1002n, are formed in a dielectric layer 1011 which is attached to the main body 1010 of the flexible interconnect layer 1001. The dielectric layer 1011 serves to electrically isolate the row interconnects and to have a flat, planar surface. Alternatively, the row interconnects may be formed on the surface of the main body 1010 such that they protrude from the surface. The dielectric layer may be formed from a photoresist which is patterned to create grooves for the row interconnects which are then deposited into grooves. A via 1009 is shown in the main body 1010 in **Figure 7J**. This via 1009 is illustrated in dashed lines because it is not present in the cross-section at line 7J-7J of **Figure 7I**, but rather this via is behind this cross-section. This via 1009 provides an opening for an electrical interconnection between the row interconnect 1002a on one side of the tape's main body 1010 to the other side of the tape's main body 1010. A conductive post in the via 1009 provides the terminal 1003a which is electrically coupled to the row interconnect 1002a. Similarly, each row interconnect is coupled to a post in a via (not shown) in

order to provide row select signals from the post, through the main body 1010 of the tape 1001, and to the row interconnects.

Figures 8A – 8D show another embodiment of the invention in which interconnect is deposited first on the flexible web material followed by deposition of blocks. **Figure 8A** shows a planar side view of web material 59. **Figure 8B** shows recessed regions in the web material 59. **Figure 8C** shows a gross interconnect deposited onto the web material 59. **Figure 8D** shows the device of **Figure 8C** with a layer of a fine interconnect deposited on top of the layer of gross interconnect. A dielectric layer may separate the fine and gross interconnects such that they are electrically isolated. In some embodiments, only one interconnect layer is deposited onto the web material before the blocks are deposited. **Figure 8E** shows a plurality of blocks deposited (*e.g.*, by an FSA process) onto the interconnect that is coupled to the web material 59. Although a preferred embodiment is to first deposit gross interconnect onto a web material (or a substrate), another embodiment is to first place fine interconnect followed by gross interconnect onto the web material (or substrate). While the side views of **Figures 8A-8E** suggest that the fine and gross conductive interconnect layers (*e.g.* patterned traces) appear to overlap/overlay each other and hence make electrical contact, they do not have to overlap and make electrical contact and often they will not. Rather the gross interconnect layer may be deposited first to create a first pattern (to create traces on the flexible substrate 59) and then the fine interconnect layer is deposited next to create a second pattern, and the traces of the two patterns may interconnect at certain points where required for the electrical circuit. Thus, it will be appreciated that the views of **Figures 8A-8E** do not necessarily represent that the two interconnect layers will overlap, although they will normally overlap where the two layers are in electrical contact. It will also be appreciated that a single interconnect layer may be used with the embodiment of **Figures 8A-8E**. It will be understood that the terms gross interconnect and fine interconnect refer to the difference in line width of the traces and/or spacing and/or pitch of the traces in the two types of

interconnect. Typically, the traces of a fine interconnect have narrower line widths and they are spaced closer together (a tighter pitch) than the traces of a gross interconnect. A fine interconnect may be used to interconnect smaller devices (*e.g.* small FETs) in the block 14 on a substrate while the gross interconnect may be used to interconnect larger devices or conductive elements (*e.g.* pixel electrodes). **Figure 8F** shows an example of an assembly having blocks deposited (*e.g.* through an FSA process) into the recessed regions on the interconnect layers which have been deposited into recessed regions in the flexible web material 59. A substrate is optionally placed onto the blocks and interconnect layers.

Figures 9A – 9F show one embodiment of the invention wherein blocks are placed onto the web material followed by single or multiple layers of interconnect. **Figure 9A** shows a planar side view of web material 59. **Figure 9B** shows a planar side view of web material 59 having recessed regions or holes therein. These recessed regions or holes may be created by a variety of methods. **Figure 9C** shows a planar view of web material 59 wherein the blocks are seated in the recessed regions or holes. The blocks comprise in one embodiment an active circuit element (not shown) which drives a picture element (not shown). **Figure 9D** shows a planar view of web material 59 of **Figure 9C** wherein an interconnect is deposited onto the web material 59. This interconnect 65 may be comprised of copper, aluminum, or other conductive material listed above. Numerous methods of depositing interconnect are described in more detail below. Although fine interconnect is shown, gross interconnect may be used in place of fine interconnect or gross interconnect could be deposited onto the web material followed by a dielectric layer and then followed by a layer of fine interconnect.

Figure 10 shows one method of assembling a flexible display along the length of a flexible substrate 70A in accordance with an embodiment of the invention. Initially, blocks are assembled into the openings of the flexible

substrate. Utilizing an FSA process, a plurality of blocks are deposited in a slurry and blocks go into the recessed regions of a substrate. Planarization of the assembly of blocks into substrate 72 is the next operation. Extrusion bar coating is one of many methods that may be used to planarize web material. The blocks may then be electrically interconnected using a flexible interconnect layer in operation 74. The display may then be coupled to a substrate in operation 76. The display can be made to conform the object's shape in operation 78. Operations for forming the display may be done in a different order than that found in **Figure 10** and thus the operation 78 may be performed after operation 80. A display generation substrate (*e.g.*, a PDLC layer) is coupled to the active matrix backplane at operation 80.

Figure 11 shows a method of manufacturing multiple displays along a flexible substrate as in a web process. Multiple display components are created on a flexible substrate at operation 200. Interconnect is deposited on web material. Interconnect may be deposited by a variety of methods such as screen printing, laser etching, or dropping display material from container. The flexible substrate is advanced to a second region on the substrate at operation 202. A new display component is created on the flexible substrate in a different region of the substrate at operation 204 by advancing the flexible substrate through a web processing of apparatus at operation 206 and coupling a display material to the substrate at operation 208. Separation of the display panel occurs at the end of the process at operation 210.

Figures 12A – 12B show another embodiment of the invention in which a reflective display is assembled. **Figure 12A** shows a flexible reflective display. Blocks 14 are coupled to the substrate 59 and to the flexible interconnect layers 1245 and 1248. As in the case of **Figure 8D**, the layers 1245 and 1248 do not have to overlap as shown in **Figure 12A** except where desired for an electrical interconnect. Coupled to the flexible substrate 59 is a flexible reflector 1247. **Figure 12B** shows a flexible reflective display wherein recessed

regions contain reflective material 1264. It should be noted that a flexible interconnect layer 1245 could be placed between the plurality of blocks and substrate 59. Interconnect may be fine, gross, or both.

Figure 13 shows a method of fabricating a display device wherein a substrate 50 and a substrate undergo processing and are subsequently coupled. There, the substrate 50 is advanced along a process line at operation 500. A slurry containing a plurality of blocks is dispensed onto a substrate at operation 502. A second slurry containing a plurality of blocks is again dispensed onto the substrate. Excess slurry is collected in a container and is recycled. The blocks fall into recessed regions into the substrate. Adhesives and spacers are deposited onto the substrate at operation 504. Display material is placed onto the substrate at operation 508. This material may comprise polymer-dispersed liquid crystal, cholesteric liquid crystal, electrophoretic liquid crystal, upconverting phosphor, or downconverting phosphor.

Figure 14 shows the overall process of fabricating a display device wherein a web material 120 and a display tape 160 undergo processing separately and are subsequently coupled. There, the web material is advanced along a first process line and advances through a first set of support members 122. A first slurry 124 containing a plurality of blocks is dispensed onto the substrate. A second slurry 126 containing a plurality of blocks is again dispensed onto the substrate. Excess slurry is collected in a container 128 and is recycled. The blocks fall into recessed regions in the substrate. Substrate 120 is advanced through a second set of support members 130. An interconnect 132 is then deposited onto the substrate 120. In one embodiment, the interconnect may be a flexible tape which is created in a separate web process, where this tape is joined to the substrate 120. The substrate is then advanced to point 134. In conjunction with this process, display tape 160 undergoes a separate process. Display material is placed onto at least one side of the display tape 160. Display tape 160 is advanced through a first set of support members 164. The display

material is patterned or layered at point 168. This display material may comprise polymer-dispersed liquid crystal, cholesteric liquid crystal, electrophoretic liquid crystal, upconverting phosphor, or downconverting phosphor. Display tape 160 is advanced through a second set of support members 170. An interconnect 172 is either deposited or etched onto the display tape 160. The display tape is then advanced to point 134 where the display tape is coupled to the substrate. This assembly (the combination of the processed substrate 120 and the display tape 160) is then coupled to a rigid or flexible substrate. A conveyor belt 174 surrounds the support members.

Figure 15 relates to a method of picking and placing of objects onto a substrate after the FSA process has been applied to the substrate. A slurry containing a plurality of objects is dispensed onto the substrate at operation 90. The objects fall into recessed regions in the substrate. The excess slurry is collected and recycled at operation 91. The substrate is checked for empty recessed regions at operation 92. This checking is performed by a camera which views the substrate. Objects are robotically placed into empty regions found in substrate at operation 94. A metalization material is placed onto at least one of the substrate's surfaces and is patterned or etched at operation 96. The display tape is coupled to the substrate at operation 98.

Figure 16 shows an embodiment of the overall in-line process of the invention. A web apparatus machine 119 is used to process the substrate. At operation 120, the material is unrolled and apertures are created in the substrate. These apertures can be created by a number of methods. For example, the apertures can be punched into the substrate. Another method involves using a template to create the apertures. A laser could also be used to create the apertures. The substrate advances over a plurality of support members 122. The FSA process is applied to the web material. FSA comprises a slurry which contains a plurality of functional blocks. These blocks have, in one embodiment, a circuit element (not shown) which drives the picture element (not shown). The

FSA process occurs at block 124. It is then applied again at 126. The excess slurry is collected in container 128. Then, the substrate advances through support members 130. The substrate then has an interconnect 131 deposited on the top of the flexible substrate 132. The resulting flexible substrate advances over a guide member and meets at a point 134 wherein it is coupled to a display tape which in one embodiment is a flexible substrate which includes separate regions each having a display material on this flexible substrate. A different portion of the process involves the display tape 160. Before the display tape is coupled with the substrate, the display tape goes through its own separate process which is described below.

The display tape has display material 162 deposited on at least one side of the display tape. There are a variety of ways that display material may be deposited onto the display tape. For example, display material may be sprayed onto the display tape; the display material also may be placed on a screen over the display tape; or the display tape may be placed into a container which holds the display material. The display tape advances through support members 164. The display tape then has display material layered or patterned on the display tape at 168. This display tape then advances through another plurality of support members 170. A large area metal interconnect is then deposited or etched onto the display tape 172. This may be performed by inkjet, lithography and etch, screen print, laser etch, or deposit. In one embodiment of the invention, this large interconnect is a cover glass electrode. At point 134, the display tape is coupled with a substrate.

Figure 17 shows a display material being placed through a screen 180 onto display tape 168. The screen 180 has a desired pattern created by holes which go through the screen 180. This desired pattern may be dictated by a customer or by the manufacturer.

Another method of placing display material onto the display tape is shown in **Figure 18**. **Figure 18** shows a top view of display material being laser

etched onto display tape 168. The etching occurs when the high intensity light from the laser 182 strikes the display material on top of the display tape 168. A pattern is created in the display material by the laser 182.

Another method of depositing display material is shown in **Figure 19**. **Figure 19** shows lithography being used to pattern the display material. Lithography involves using a block 183 with a pattern engraved in the bottom surface of the block 183. The bottom surface of the block 183 contacts the display material.

Figure 20 shows yet another method of depositing display material onto the display tape. There, display material is deposited in a pattern onto the display tape 168. The display material is deposited by a container 184 which contains the display material. The container 184 is placed over the display tape 168. The display material drops onto the display tape 168 in a pattern.

While an array of components (e.g. display components) for an assembly have been described as examples of the invention, an array of other assemblies such as x-ray detectors, radar detectors, micro-electro-mechanical structural elements (MEMS) or, generally, an assembly of sensors or actuators or an assembly of circuit elements also may be produced using the claimed invention. Thus, for example, flexible antennas, other sensors, detectors, or an array of circuit elements may be fabricated using one of the embodiments of the inventions. Other aspects and methods of the present invention as well as apparatuses formed using these methods are described further below in conjunction with the following figures.

Listed below are related U.S. Patent Applications that describe various improvements to the methods and devices of the invention described herein. These patent applications and a U. S. Patent are incorporated by reference.

Co-pending U.S. Patent Application Serial No. _____, entitled "*Apparatuses and Methods for Forming Assemblies*," (Docket No.

-22-

003424.P008), filed by Jeffrey J. Jacobsen and assigned to the same Assignee as the present invention, describes a method and apparatus of assembling flexible displays. This co-pending application is hereby incorporated herein by reference.

Co-pending U.S. Patent Application Serial No. _____, entitled "*Methods for Transferring Elements From A Template To A Substrate*" (Docket No. 003424.P009), filed by Jeffrey J. Jacobsen, Mark A. Hadley, and John Stephen Smith and assigned to the same Assignee of the present invention, describe an FSA on a template with transfer to another substrate. These co-pending applications are hereby incorporated herein by reference.

Co-pending U.S. Patent Application Serial No. _____, entitled "*Methods and Apparatuses for Fabricating A Multiple Module Assembly*" (Docket No. 003424.P010), filed by Jeffrey J. Jacobsen, Glenn Wilhelm Gengel, and Gordon S.W. Craig and assigned to the same Assignee as the present invention, describes an electronic modular assembly. This co-pending application is hereby incorporated herein by reference.

Co-pending U.S. Patent Application Serial No. _____, entitled "*Apparatuses and Methods Used in Forming Electronic Assemblies*" (Docket No. 003424.P011), filed by Jeffrey J. Jacobsen, Glenn Wilhelm Gengel, and John Stephen Smith and assigned to the same Assignee as the present invention, describes a method of molding substances. This co-pending application is hereby incorporated herein by reference.

Co-pending U.S. Patent Application Serial No. _____, entitled "*Apparatuses and Methods for Forming Assemblies*" (Docket No. 003424.P016), filed by Jeffrey J. Jacobsen and assigned to the same Assignee as the present invention, describes a method of rolling blocks into their recessed regions. This co-pending application is hereby incorporated herein by reference.

Patent No. 5,545,291 entitled "*Method for Fabricating Self-Assembling Microstructures*," filed by John S. Smith and Hsi-Jen J. Yeh, issued August 13, 1996.

In the preceding detailed description, the invention is described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A method of fabricating an electronic assembly, said method comprising:
providing a substrate with a plurality of blocks each of which includes at least one functional component;
applying an electrical interconnect layer onto a flexible layer;
attaching said flexible layer to said substrate;
electrically coupling said electrical interconnect layer to at least one of said blocks.
2. The method of claim 1, wherein said at least one functional component is an electrical component and wherein said blocks are fabricated separately from said substrate and are deposited onto said substrate.
3. The method of claim 1, wherein said substrate is flexible and said blocks are deposited onto recessed regions of said substrate.
4. The method of claim 3, wherein said substrate is attached to said flexible layer in a web process apparatus.
5. The method of claim 1, wherein the flexible layer is selected from the group consisting of polyether sulfone, polyethylene terephthalate, polycarbonate, polybutylene terephthalate, polyphenylene sulfide, polypropylene, polyester, aramid, polyamide-imide, polyimide, aromatic polyimides, polyetherimide, metallic materials, acrylonitrile butadiene styrene, polyvinyl chloride, polyamide, nylon, polybutylene naphthalate, polyethylene naphthalate, polybutylene naphthalate, and polycycloolefins.

-25-

6. The method of claim 1, wherein a slurry containing said plurality of blocks is deposited onto the flexible layer.
7. The method of claim 1, wherein the blocks are transferred to said substrate by pressing a template having said blocks into the substrate.
8. The method of claim 3, wherein the blocks are robotically placed into empty recessed regions.
9. The method of claim 1, further comprising applying interconnect onto the web material by laser.
10. The method of claim 1, further comprising applying interconnect onto the flexible layer by photolithography.
11. The method of claim 1, further comprising applying interconnect onto the flexible layer by screen printing.
12. The method of claim 1, further comprising applying interconnect onto the flexible layer by ink jet processes.
13. The method of claim 1, further comprising applying interconnect onto the flexible layer by ultraviolet light.
14. The method of claim 1, further comprising transferring a plurality of blocks to a flexible layer by a template.
15. The method of claim 1, wherein the electrical interconnect layer is selected from the group consisting of aluminum, copper, silver, and gold.

-26-

16. An electronic assembly comprising:
 - a substrate having a plurality of blocks which are deposited onto receptor regions of said substrate, each of said blocks including at least one functional component and at least one electrical terminal;
 - a flexible layer attached to said substrate, said flexible layer comprising an electrical interconnect layer;
 - wherein said electrical interconnect layer is coupled to said at least one electrical terminal.
17. An electronic assembly as in claim 16 wherein said at least one functional component is an electrical component and said blocks are fabricated separately from said substrate and are deposited onto said substrate.
18. An electronic assembly as in claim 16 wherein said substrate is flexible and is attached to said flexible layer in a web process.
19. An electronic assembly as in claim 16 wherein said electrical interconnect layer is attached to said flexible layer in a web process.
20. An electronic assembly as in claim 16, wherein electrical interconnect layer is a fine interconnect.
21. An electronic assembly as in claim 16, wherein electrical interconnect layer is a gross interconnect.
22. An electronic assembly as in claim 16, wherein the electrical interconnect layer is selected from the group consisting of aluminum, copper, silver, and gold.
23. A method of fabricating an electronic assembly, said method comprising:

-27-

providing a flexible layer with a plurality of blocks each of which includes at least one functional component;

applying an electrical interconnect layer onto the flexible layer;

attaching said flexible layer to a substrate;

electrically coupling said electrical interconnect layer to at least one of said blocks.

24. The method of claim 23, wherein the flexible layer includes the material selected from the group consisting of aluminum, copper, silver, gold, metal, polyether sulfone, polycarbonate, polybutylene terephthalate, polyphenylene sulfide, polypropylene, polyester, aramid, polyamide-imide, polyimide, aromatic polyimides, polyetherimide, acrylonitrile butadiene styrene, polyvinyl chloride, polyamide, nylon, polybutylene naphthalate (PBN), polyethylene naphthate, polybutylene naphthalate, and polycycloolefins.

25. The method of claim 23, wherein the flexible layer is reflective.

26. A method of fabricating an electronic assembly, said method comprising:
applying an electrical interconnect layer onto a flexible layer;
dispensing onto the flexible layer a plurality of blocks each of which includes at least one functional component;

attaching said flexible layer to a substrate;

electrically coupling said electrical interconnect layer to at least one of said blocks.

27. The method of claim 26, wherein the flexible layer includes the material selected from the group consisting of aluminum, copper, silver, gold, metal, polyether sulfone, polycarbonate, polybutylene terephthalate, polyphenylene sulfide, polypropylene, polyester, aramid, polyamide-imide, polyimide, aromatic polyimides, polyetherimide, acrylonitrile butadiene styrene, polyvinyl chloride,

-28-

polyamide, nylon, polybutylene naphthalate (PBN), polyethylene naphthalate, polybutylene naphthalate, and polycycloolefins.

28. The method of claim 26, wherein the flexible layer is reflective.

29. The method of claim 26, wherein the assembly has an OLED.

1/18

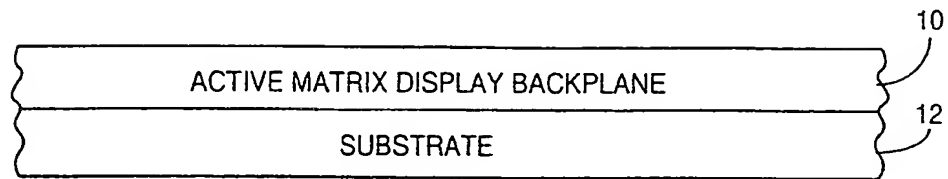


Fig. 1a
(Prior Art)

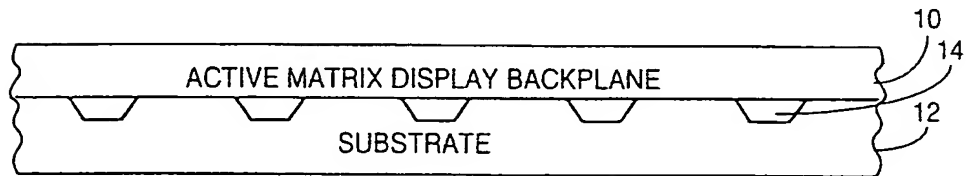


Fig. 1b
(Prior Art)

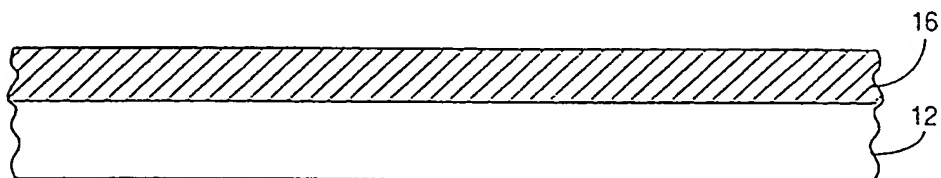


Fig. 1c
(Prior Art)

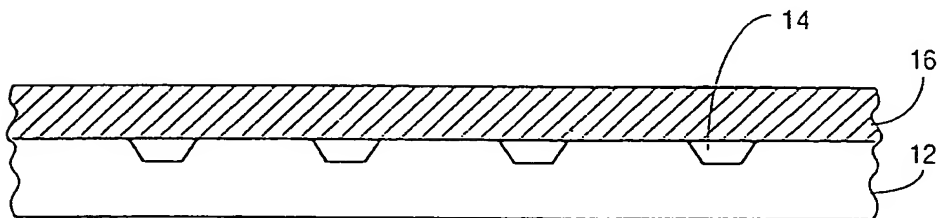


Fig. 1d
(Prior Art)

2/18

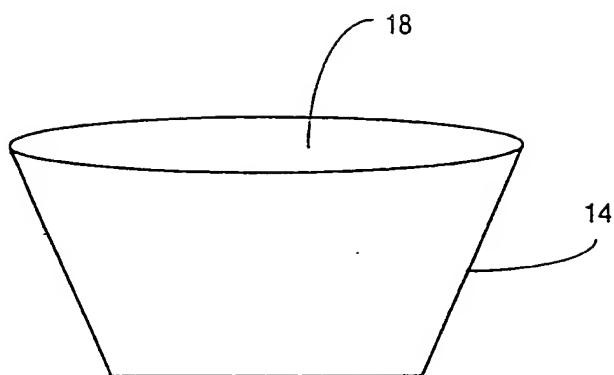


Fig. 2
(Prior Art)

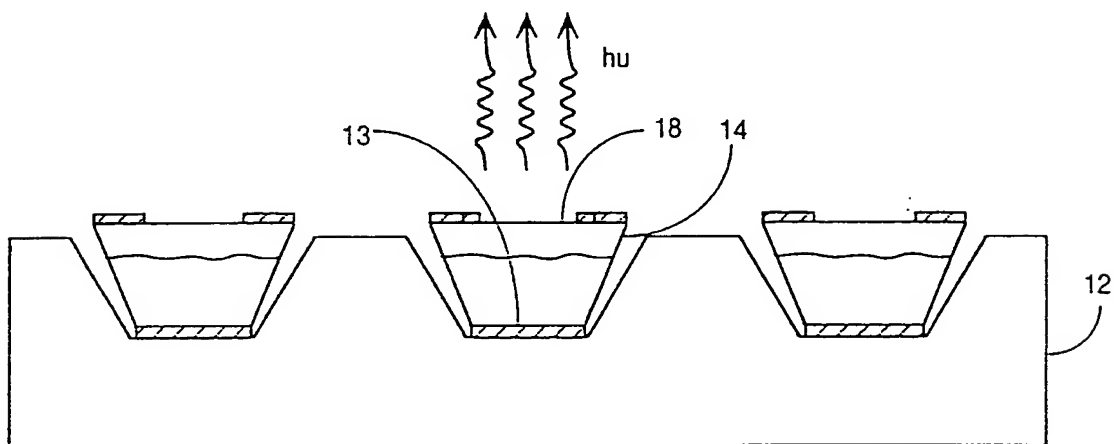


Fig. 3
(Prior Art)

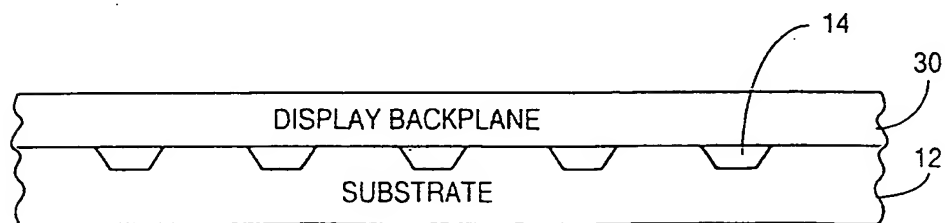


Fig. 4
(Prior Art)

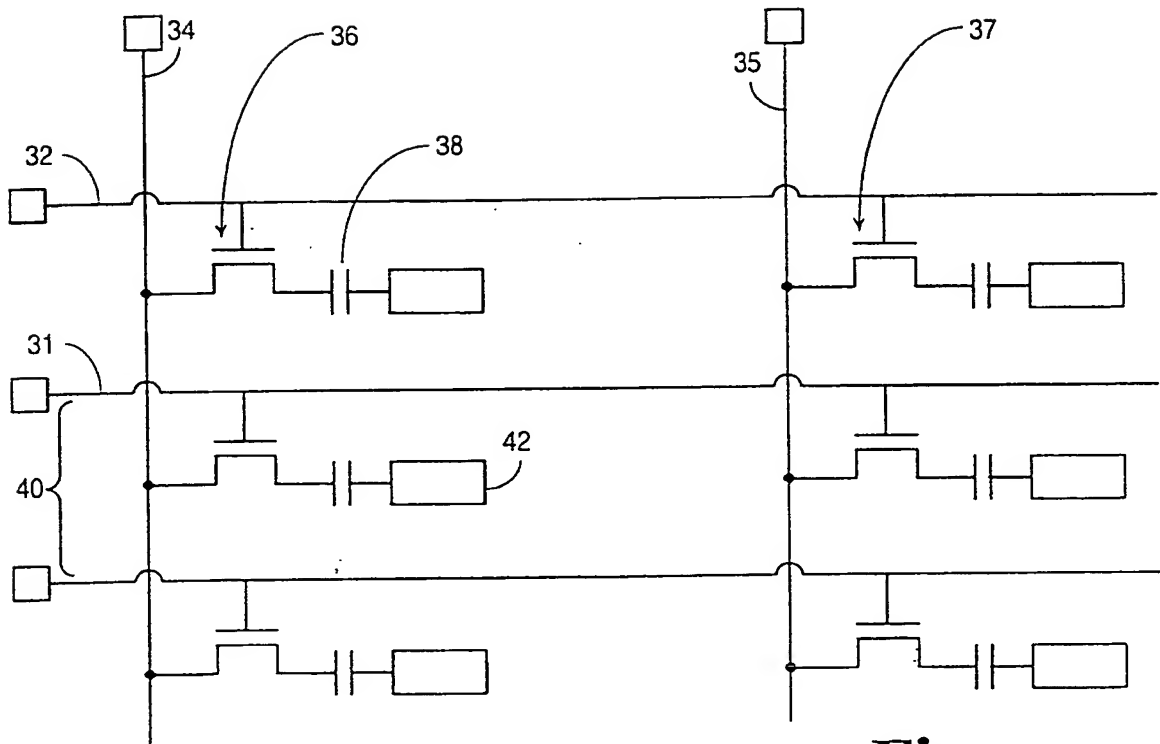


Fig. 5
(Prior Art)

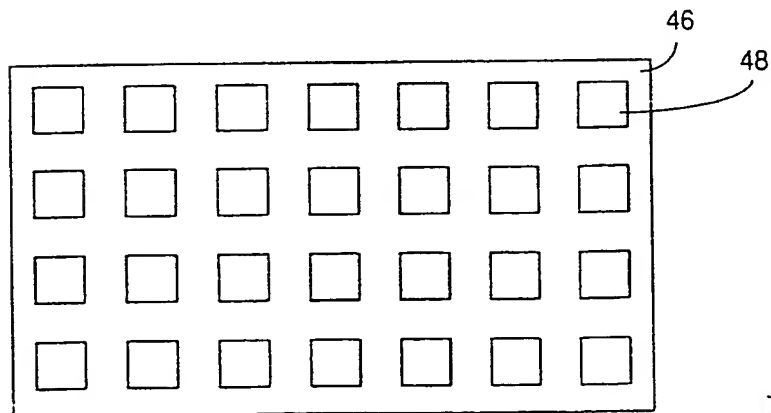


Fig. 6
(Prior Art)

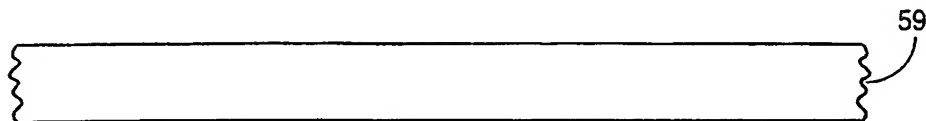


Fig. 7A

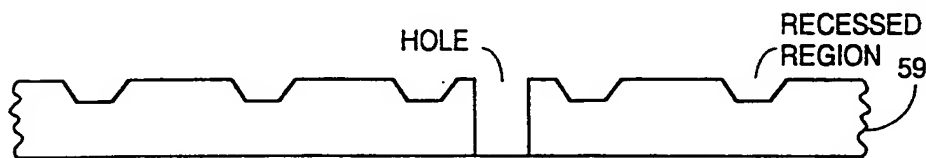


Fig. 7B

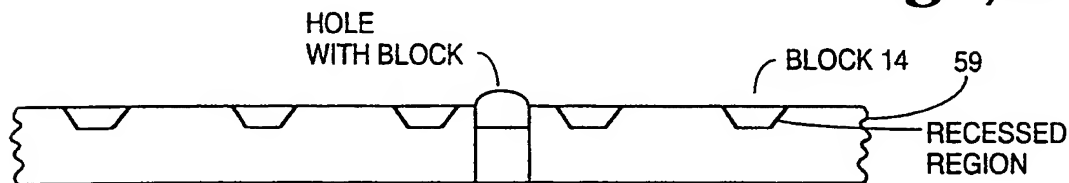


Fig. 7C

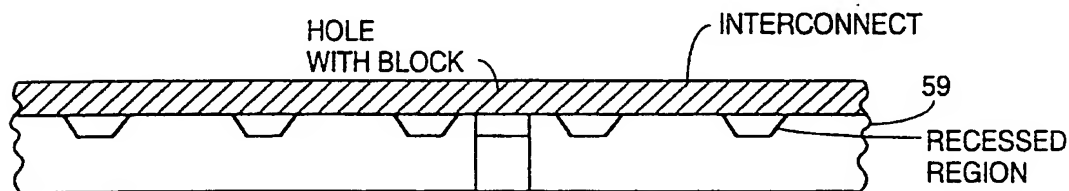


Fig. 7D

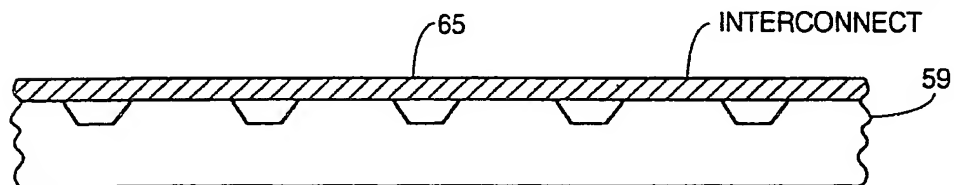


Fig. 7E

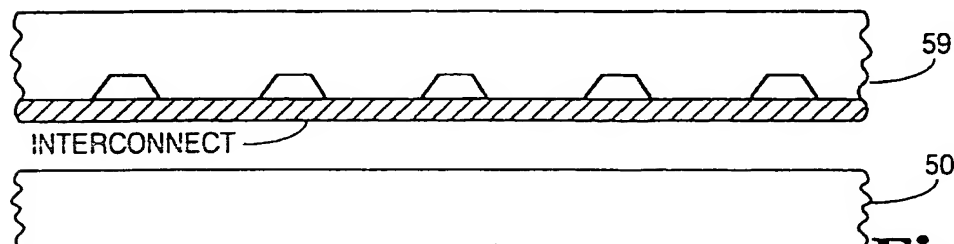
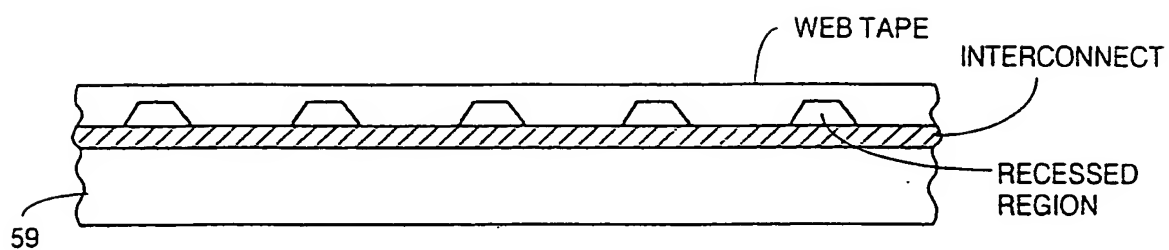
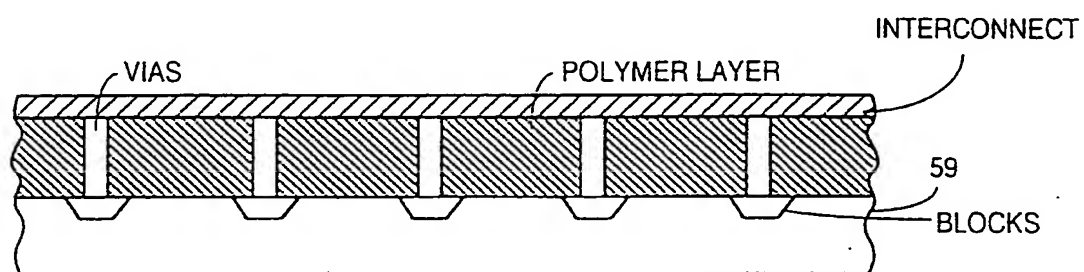


Fig. 7F

5/18

**Fig. 7G****Fig. 7H**

7/18

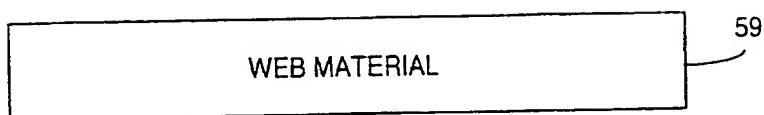


Fig. 8A

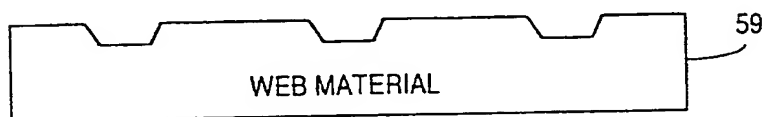


Fig. 8B

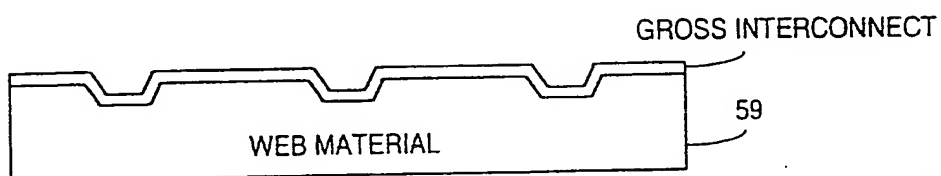


Fig. 8C

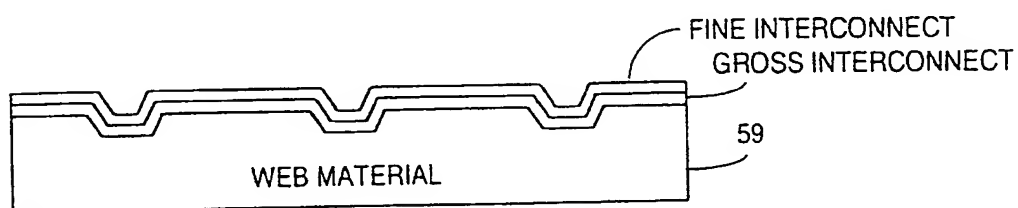


Fig. 8D

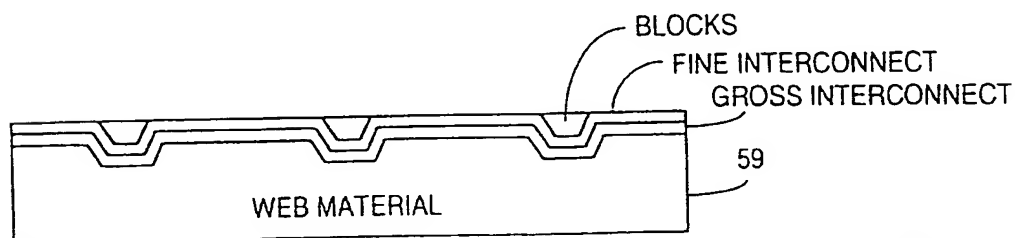


Fig. 8E

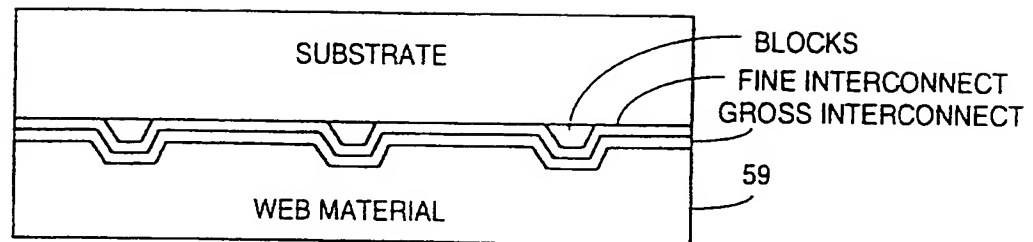


Fig. 8F

9/18

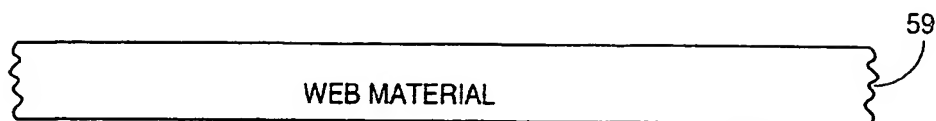


Fig. 9A

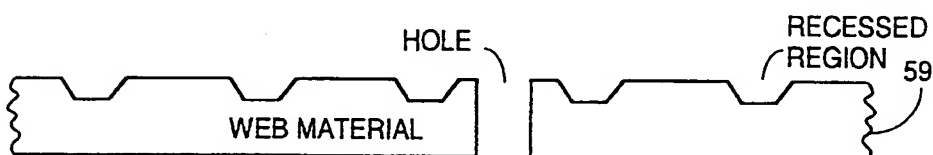


Fig. 9B

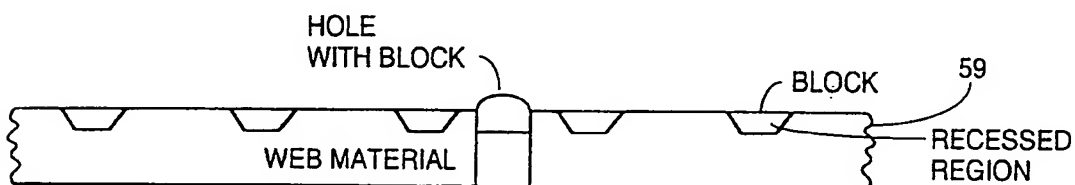


Fig. 9C

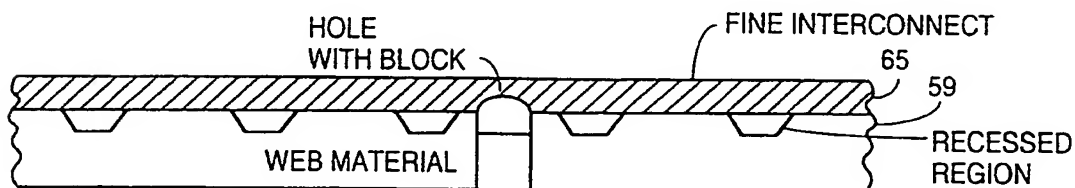
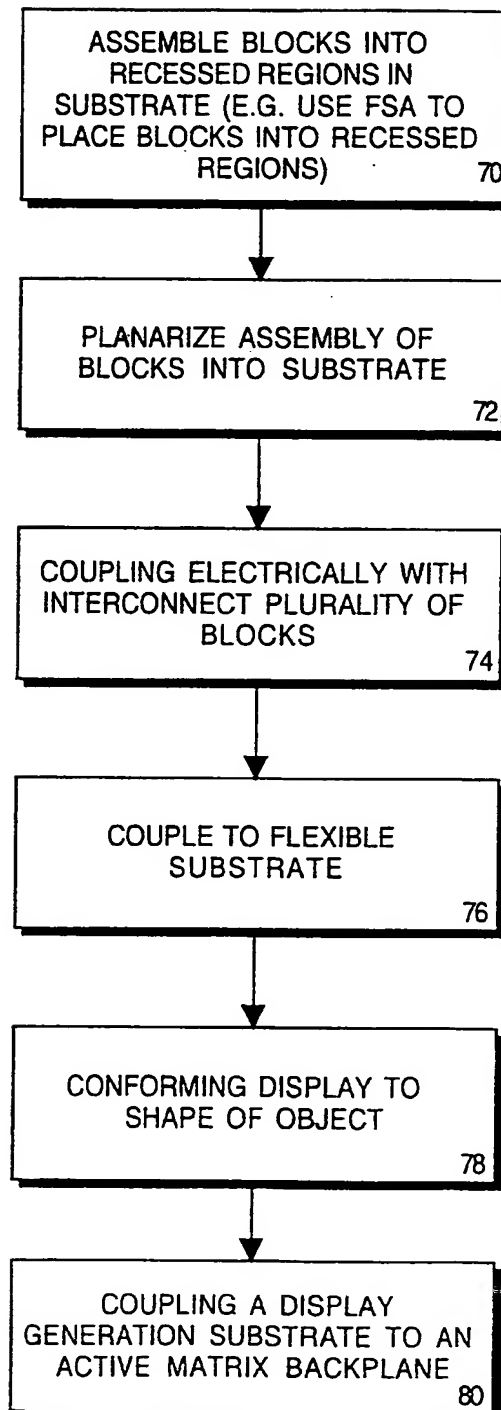
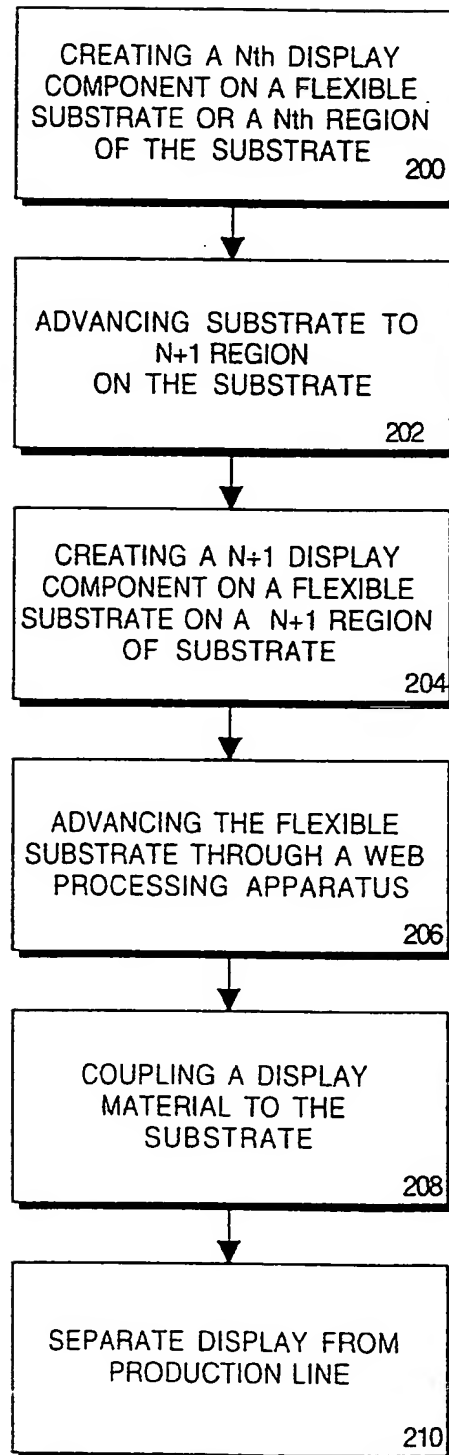


Fig. 9D

10/18

**Fig. 10**

11/18

**Fig. 11**

12/18

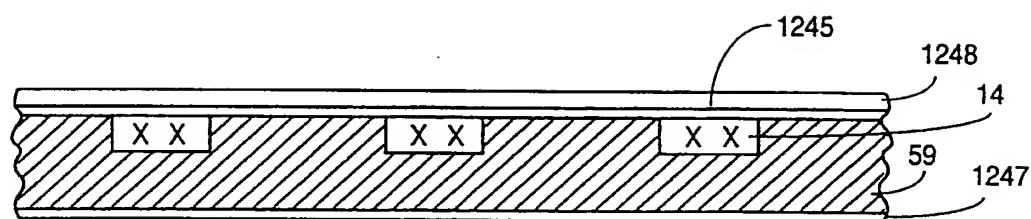


Fig. 12A

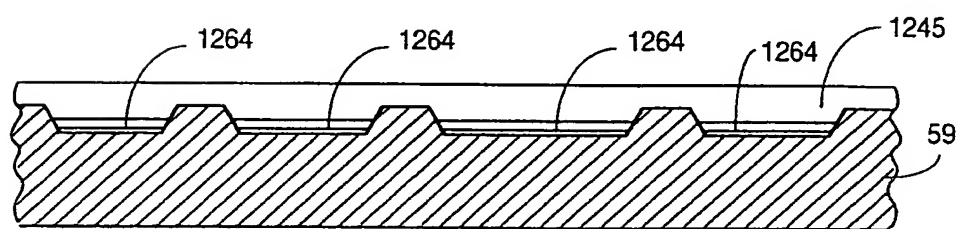
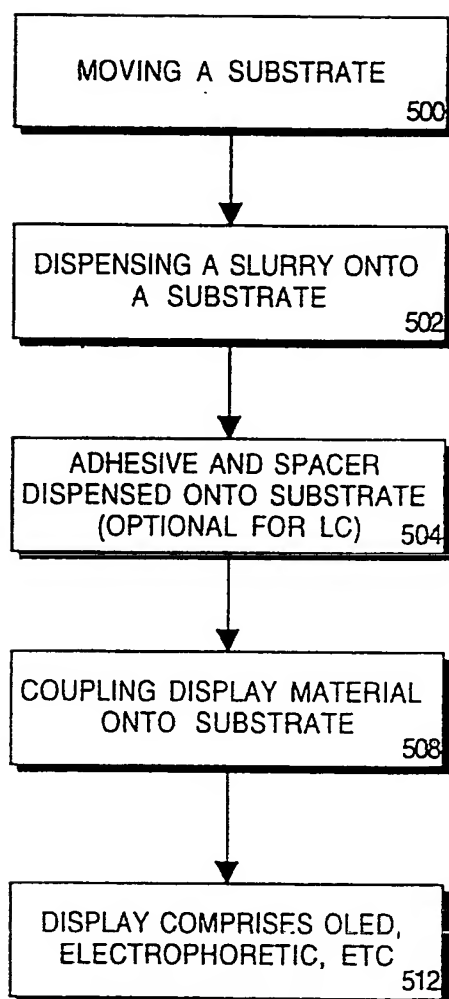


Fig. 12B

13/18

**Fig. 13**

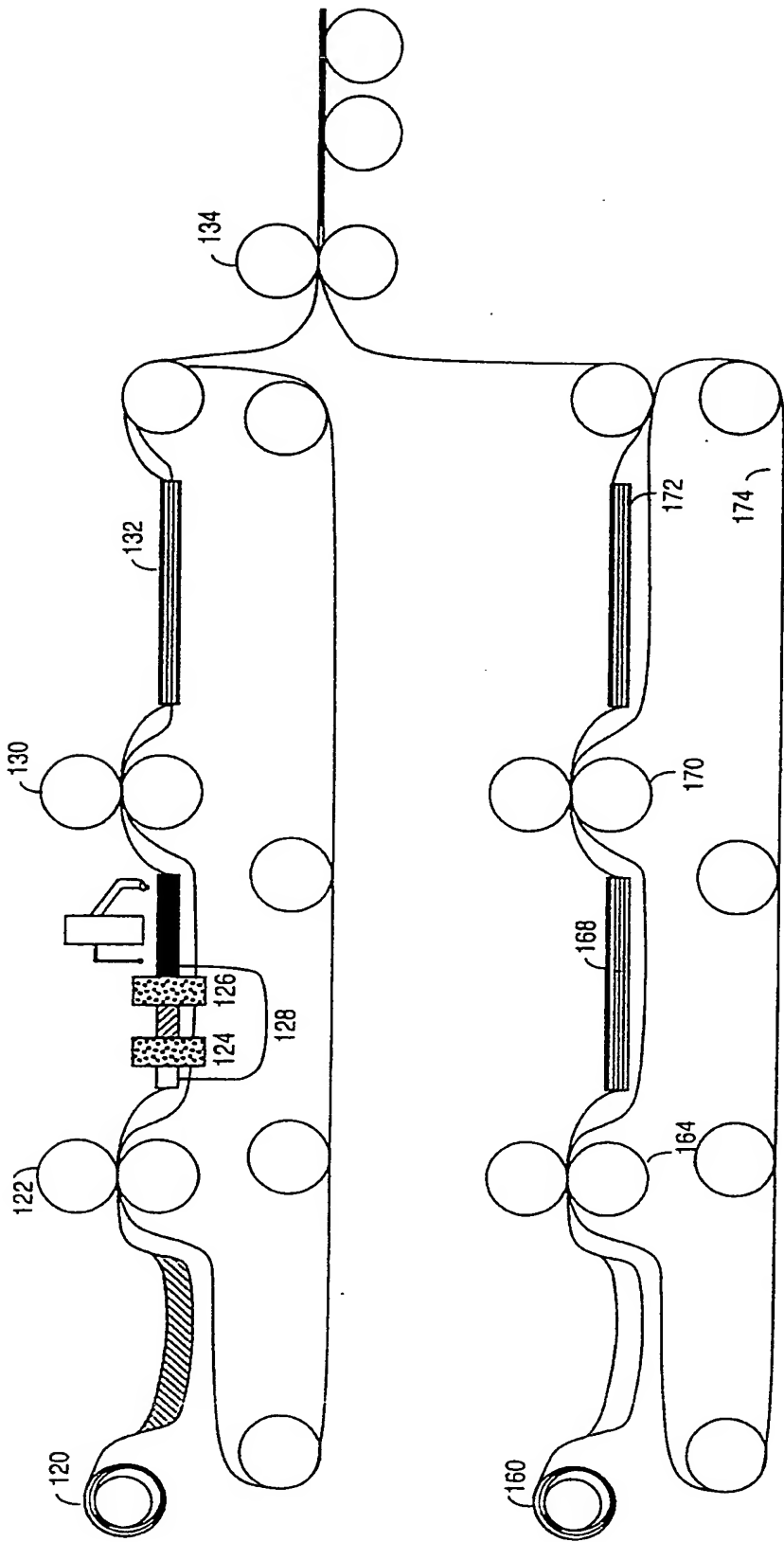


Fig. 14

15/18

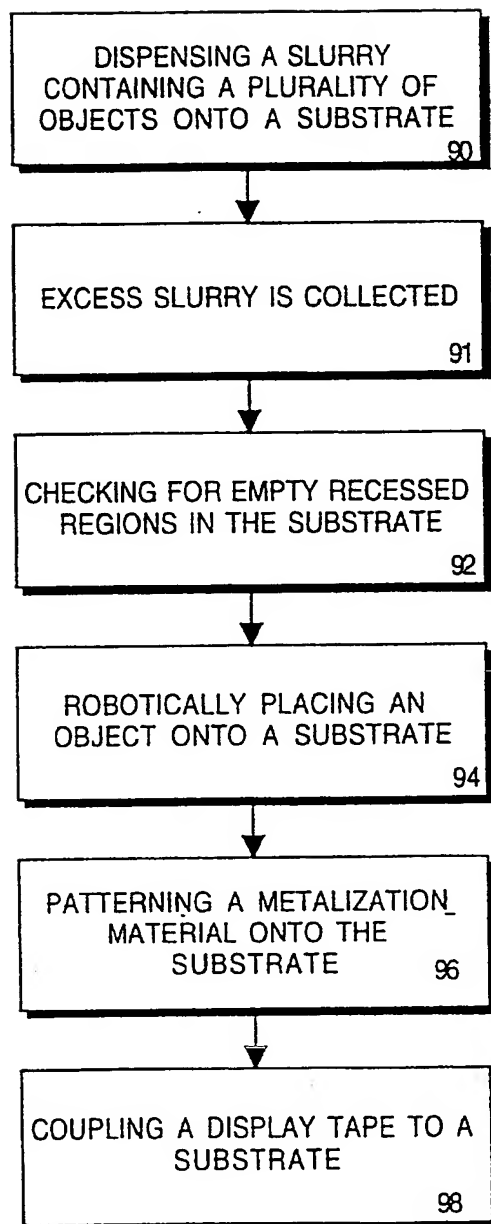


Fig. 15

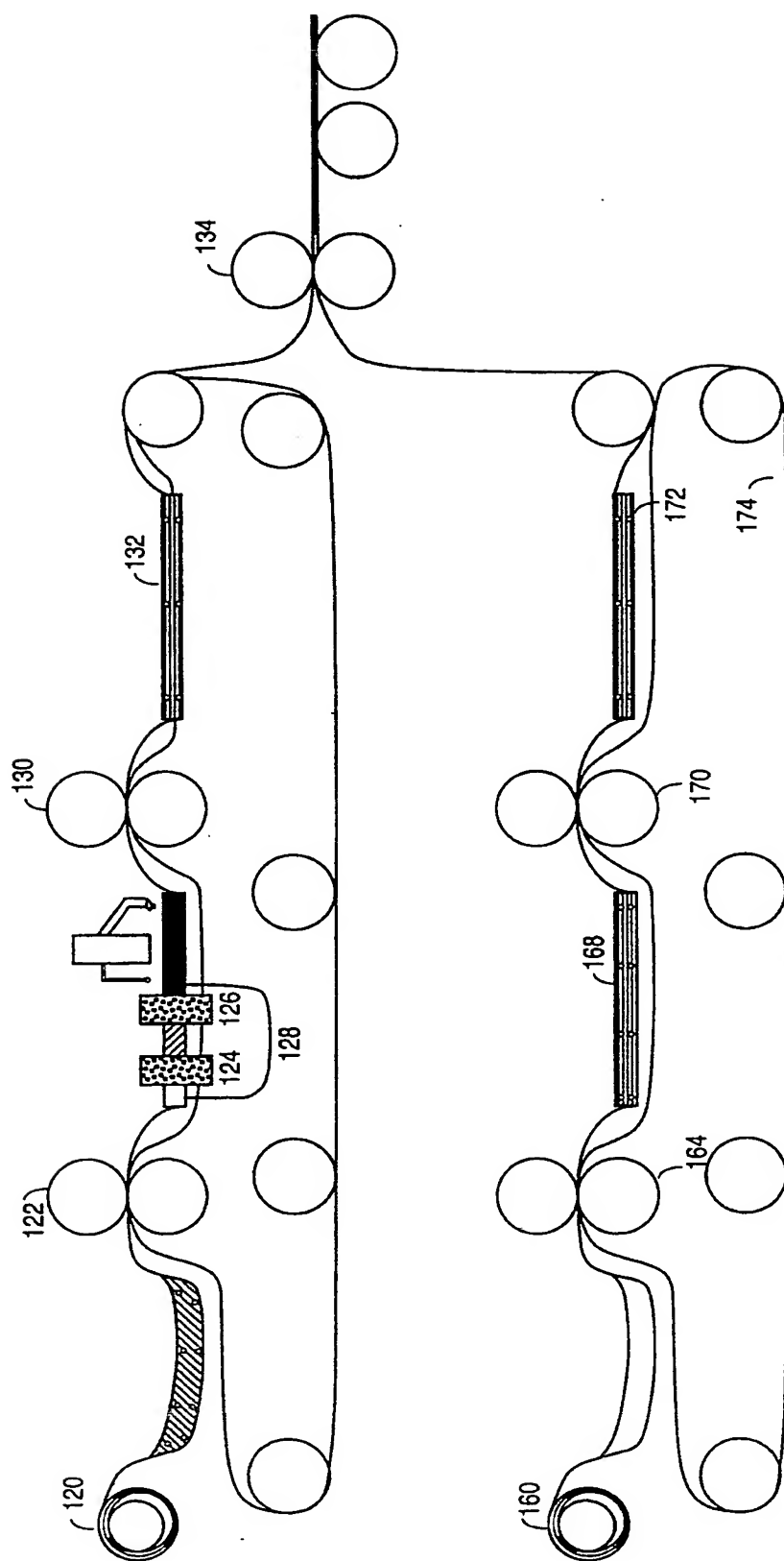


Fig. 16

17/18

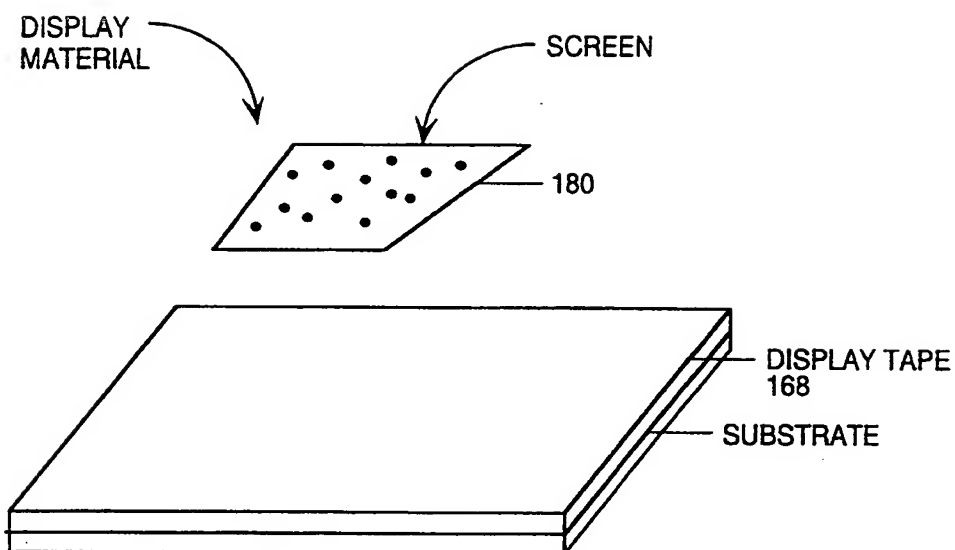


Fig. 17

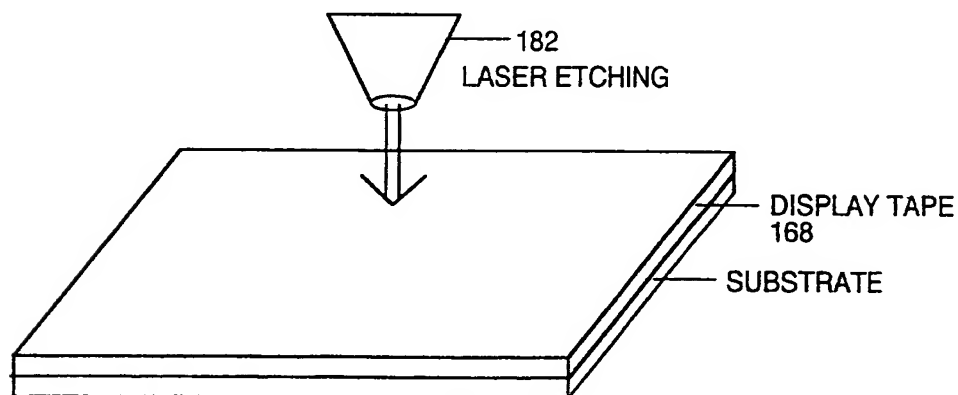


Fig. 18

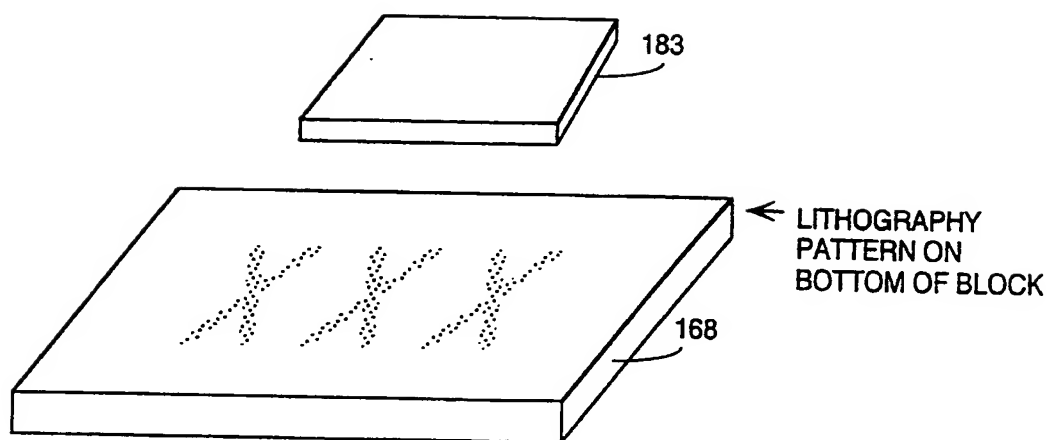


Fig. 19

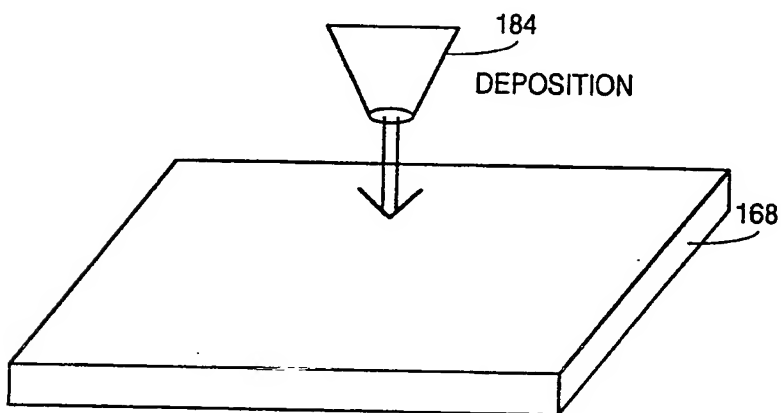


Fig. 20

INTERNATIONAL SEARCH REPORT

International Application No.
PCT/US 00/02348

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L23/538 H01L21/98

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 450 950 A (GEN ELECTRIC) 9 October 1991 (1991-10-09) the whole document	1-5, 9, 10, 13, 15-24, 26, 27
X	US 5 138 433 A (HIRUTA YOICHI) 11 August 1992 (1992-08-11) the whole document	1, 16, 23, 26
X	DE 28 10 054 A (MATSUSHITA ELECTRIC IND CO LTD) 14 September 1978 (1978-09-14) the whole document	26
A	US 3 903 590 A (YOKOGAWA SYUNZI) 9 September 1975 (1975-09-09) the whole document	7
	--- -/-	

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

26 April 2000

Date of mailing of the international search report

04/05/2000

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Prohaska, G

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/02348

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 498 703 A (FRANCE TELECOM) 12 August 1992 (1992-08-12) the whole document ----	8
A	EP 0 277 606 A (IBM) 10 August 1988 (1988-08-10) the whole document ----	1-29
A	WO 88 02549 A (GEN ELECTRIC) 7 April 1988 (1988-04-07) -----	

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 00/02348

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
EP 0450950	A	09-10-1991	JP 4251968 A	08-09-1992
			US 5452182 A	19-09-1995
US 5138433	A	11-08-1992	JP 2054531 C	23-05-1996
			JP 3268351 A	29-11-1991
			JP 7077258 B	16-08-1995
DE 2810054	A	14-09-1978	JP 1192560 C	29-02-1984
			JP 53110370 A	27-09-1978
			JP 58026667 B	04-06-1983
			JP 1253425 C	26-02-1985
			JP 53124976 A	31-10-1978
			JP 59029145 B	18-07-1984
			JP 53139972 A	06-12-1978
			JP 1183049 C	27-12-1983
			JP 54048074 A	16-04-1979
			JP 58011113 B	01-03-1983
			JP 1174840 C	28-10-1983
			JP 54050873 A	21-04-1979
			JP 58006951 B	07-02-1983
			CA 1108305 A	01-09-1981
			GB 1588377 A	23-04-1981
			US 4356374 A	26-10-1982
			US 4246595 A	20-01-1981
US 3903590	A	09-09-1975	CA 994004 A	27-07-1976
			DE 2411259 A	19-09-1974
			FR 2220879 A	04-10-1974
			GB 1426539 A	03-03-1976
EP 0498703	A	12-08-1992	FR 2672428 A	07-08-1992
			DE 69226973 D	22-10-1998
			DE 69226973 T	11-03-1999
			JP 6112240 A	22-04-1994
EP 0277606	A	10-08-1988	US 4766670 A	30-08-1988
			DE 3888552 D	28-04-1994
			DE 3888552 T	27-10-1994
			JP 1891930 C	07-12-1994
			JP 6018247 B	09-03-1994
			JP 63196051 A	15-08-1988
			US 4855867 A	08-08-1989
WO 8802549	A	07-04-1988	DE 3777164 A	09-04-1992
			EP 0286660 A	19-10-1988
			JP 1501031 T	06-04-1989
			US 4937203 A	26-06-1990